O.K. To Enter
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JNT

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method for reducing detrimental phenomena related to disturb voltages in a data storage apparatus employing passive matrix-addressing, ~~particularly a memory device or a sensor device,~~ wherein the data storage apparatus comprises a plurality of data storage cells for storing logical values as given by a specific charge value set in each cell, wherein each of the data storage cells comprises an electrically polarizable memory material exhibiting hysteresis, ~~particularly a ferroelectric or electret material,~~ wherein the cells are physically disposed in one or more matrices, ~~wherein~~ each of said matrices providing passive matrix addressability to the cells, ~~wherein~~ and each of the matrices comprising a first and a second electrode set, ~~wherein~~ the electrodes of each set ~~are~~ provided in parallel, one set of electrodes forming word lines and the other set forming bit lines, wherein the word line electrodes and the bit line electrodes are provided crossing each other and in direct or indirect contact with the memory material, ~~wherein~~ the data storage cells of the apparatus ~~are~~ realized as capacitor-like elements defined in a volume of the memory material between or at the crossings of word lines and bit lines and ~~can be~~ settable to either of at least two polarization states ~~or switched therebetween~~ by applying an active voltage pulse of a voltage V_S larger than ~~the~~ a coercive voltage V_C corresponding to ~~the~~ a coercive electric field of the memory material, between a word line and a bit line and over the data storage cell defined therebetween, wherein an application of electric potentials conforms to an addressing operation, and wherein the electric potentials applied to all word and bit lines in the addressing operation are controlled in a time-coordinated manner according to a predetermined voltage pulse protocol,
wherein the data storage cells of the data storage apparatus are provided in two or more electrically separated segments, each segment comprising a separate physical address space of the data storage apparatus, ~~wherein~~ the method comprising:

~~a first addressing operation comprises~~ setting in a first addressing operation constituting a first part of an addressing cycle one or more addressed data storage cells in one of the segments to a first polarization state by means of a first active voltage pulse in the first addressing operation, during which each bit line dependent on the voltage pulse protocol can be connected with a sensing means for detecting the polarization state of the data storage cell at least under a part of the duration of the first active voltage pulse;

applying to the one or more addressed data storage cells in the one segment dependent on the voltage pulse protocol a second voltage pulse which can be a second active voltage pulse of opposite polarity to that of the first active voltage pulse and switching the addressed data storage cell from the first polarization state to a second polarization state, such that ~~the~~ each cell being addressed is set to a predetermined polarization state as specified by the first addressing operation; ~~characterized by further~~

applying in ~~the~~ a second addressing operation the second voltage pulse to one or more data storage cells in another segment, such that ~~the cell or~~ one or more data storage cells in the